REMARKS

The independent claims have been amended better to point out that which applicant regards as his invention. More particularly, claim 1 now specifies that (a) the wiring layer in the semiconductor device consists of a plurality of plated layers, (b) the connection members are Au wire bumps, each bump having a hemisphere portion and a longitudinal portion, and (c) a solder ball is formed on the plurality of plated layers. Claim 2 has been amended and claim 16 has been canceled in view of the changes to claim 1. Method claim 7 has been changed to specify that (a) the connection members formed on the electrodes of the respective semiconductor chips are formed by Au wire bonding, (b) those connection members are Au wire bumps, each having a hemisphere portion and a longitudinal portion, and (c) the connection members have been formed on the surfaces of the respective semiconductor chips. Claim 17 has been canceled in view of the change to claim 7. Minor, self-evident changes have been made in claims 5 and 13 also.

Applicant again requests the Examiner to respond to the Request for Approval of Drawing Change filed November 20, 2002.

The rejection of article claims 1 to 6 and 16 under 35 USC 103 as unpatentable over Miyamoto et al. '719 in view of Watase et al. '528, further in view of Matsunaga et al. '548, if applied to claims 1 to 6 is respectfully traversed (applicant notes that each reference is newly cited, the previous art rejections having been dropped).

Applicant respectfully submits that the references in combination in no proper way teach or suggest the subject matter of claims 1 to 6.

The semiconductor device of claim 1 has at least the following characteristic features:

1. the connection members extend in a direction perpendicular to the semiconductor chip, have a longitudinal shape, and have an area of contact with the wiring layer that is less than an area of contact with an electrode;

2. the connection members are Au wire bumps, each having a hemisphere portion and a longitudinal portion; and

3. the connection members are connected to a solder ball though a wiring layer on the insulating layer that consists of a plurality of plated layers. The plurality of plated layers aspect of the wiring layer is shown in the drawing at Figs. 1

and 2 and the discussion in the specification at page 9, lines 8 to 10.

As a result of the three characteristic features discussed above, because the connection members have a longitudinal shape, each with a hemisphere portion and a longitudinal portion, have an area of contact with the wiring layer that is less than an area of contact with the electrode, and are Au wire bumps, each connection member can have a longitudinal thick and soft portion consisting of an Au wire bump. With such a construction, it is unlikely that the connection members are broken even after repeated stress is applied to the connection members.

Moreover, because each connection member has an area of contact with an electrode of the semiconductor chip, the connection member can be directly and securely connected to the electrode of the semiconductor chip.

Furthermore, because the solder ball is connected to the connection member through the wiring layer consisting of a plurality of plated layers, the solder ball can be connected easily to the connection member regardless of the relative position of the solder ball and the connection member.

Lastly, because the wiring layer consists of a plurality of plated layers, the wiring layer can be easily formed and have a desired thickness. None of the newly cited references teaches or suggests these constructions or advantages to be derived therefrom.

Miyamoto et al. '719 depicts a semiconductor device having solders 11 within through holes 8a and 8b but the Miyamoto et al. '719 solders have a cylindrical shape, meaning that the solder sectional area is constant. In contrast, the connection members of the semiconductor device of claims 1 to 6 have an area of contact with the wiring layer that is less than an area of contact with an electrode and have a hemisphere portion and a longitudinal portion.

Moreover, the Miyamoto et al. '719 solder bump 9 is connected directly to the solder 11 and not through a wiring layer.

The disclosure in Watase et al. '528 does not provide what is missing in the primary reference. Watase et al. '528 discloses a wiring layer 22 that is formed by sputtering, vacuum evaporation, CVD and electroless plating; see column 11, lines 15 to 20 of the patent. If the wiring layer is made by such

techniques, that layer has a very thin foil shape and therefore is distinctly different from the connection member of the present invention.

Matsunaga et al. '548 does not have "the required connecting member configuration" as alleged in the paragraph on the bottom of page 2 of the Office Action. The reference discloses a pad 20 and a wire 23 but there is no teaching therein that an upper end of the wire 23 is connected to a wire layer consisting of a plurality of plated layers or that the solder ball is connected to the plurality of plated layers.

Applicant respectfully submits that a reading of these three references, with or without benefit of applicant's disclosure, does not lead the person of ordinary skill in the art to the configuration claimed herein. It is asserted in the paragraph at the top of page 3 of the Office Action that it would have been obvious to the person of ordinary skill in the art to combine the references "in order to have a semiconductor structure with better performance and ease of manufacturability." Applicant submits with respect that the references provide no such motivation and indeed, even with a joint consideration of the references, one is not directed to

what is claimed herein. The asserted generalizations of what the references teach do not lead the person of ordinary skill in the art to the claimed semiconductor device.

The rejection should be withdrawn.

If the rejection is maintained, the Examiner is asked to state in the record where Watase et al. '528 shows a connection member corresponding to the connection member of applicant's claims and where Matsunaga et al. '548 shows a connecting member configuration corresponding to the configuration recited in the instant claims.

The rejection of claims 7 to 15 and 17 under 35 USC 103 as unpatentable over Miyamoto et al. '719 in view of Watase et al. '528, further in view of Matsunaga et al. '548, further in view of Sasaki et al. '858, further in view of Tokishige et al. '288, further in view of Takahashi et al. '448, further in view of Fukui et al. '217, further in view of Miura et al. '697, if applied to claims 7 to 15, is respectfully traversed. Applicant respectfully submits that merely the number of references used in this rejection makes it suspect.

Applicant moreover respectfully says that the first three references do not teach or suggest the underlying article made

in accordance with this process for the reasons given above directed to the art rejection of the article claims. There is no proper rationale or analysis provided in the Office Action for combining these references. Merely reciting to what various references are said to be directed, particularly with no direction by citation to column, line or figure, cannot provide the necessary evidence in support of the rejection of these claims.

Applicant also points out that, in accordance with the present invention, the connection members are formed on the electrodes by Au wire bonding, after which the insulating layer is formed in a thickness to cover the connection members that have been formed on the electrodes. Watase et al. '528 shows a thin layer 18 being formed on the insulation layer 17 by sputtering and the like after the insulation layer is formed on the semiconductor chip 11. The references considered collectively do not teach or suggest the instantly claimed method. For these and other reasons, it is respectfully submitted that the claims patentably define over this combination of references. The rejection should be withdrawn.

In view of the foregoing amendments and remarks, it is respectfully submitted that claims 1 to 15 are in immediate condition for allowance and a USPTO paper to those ends is earnestly solicited.

The Examiner is requested to telephone the undersigned if additional changes are required in the case prior to allowance.

Respectfully submitted,

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